



THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

David Hoyle

Serial No: 09/703,140

Filed: October 31, 2000

For: Microprocessor With Rounding Multiply Instructions

Docket No.: TI-30554

Art Unit: 2124

Examiner: Mai, Tan V.

Conf. No.: 1023

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LETTER TO THE OFFICIAL DRAFTPERSON

Technology Center 2100

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(a)

I hereby certify that the above correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on March 10, 2004

Indranil Chowdhury
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Please find enclosed the formal drawings for the subject case. Charge any necessary fees to Deposit Account No. 20-0668. **This form is submitted in triplicate.**

Respectfully submitted,

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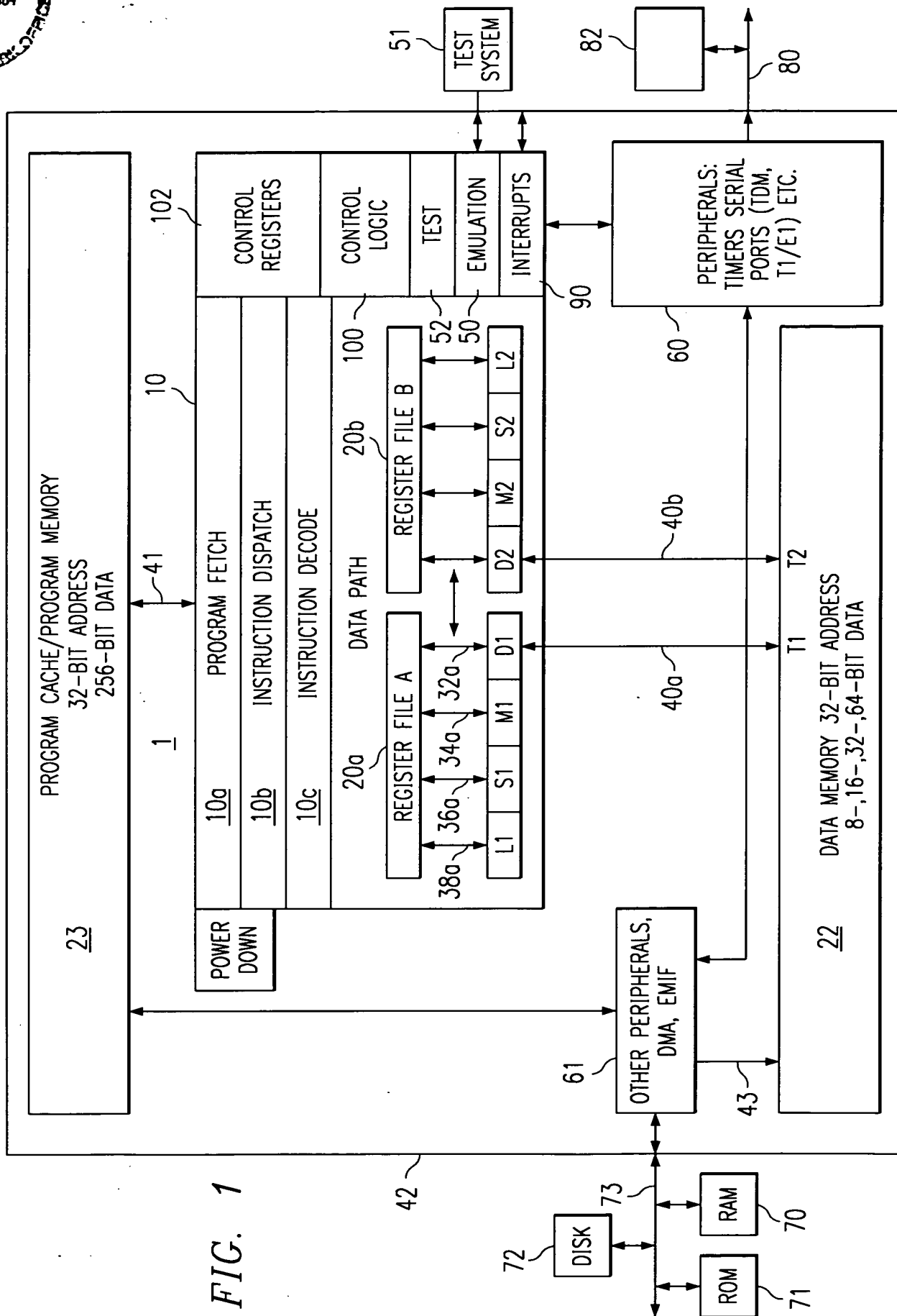
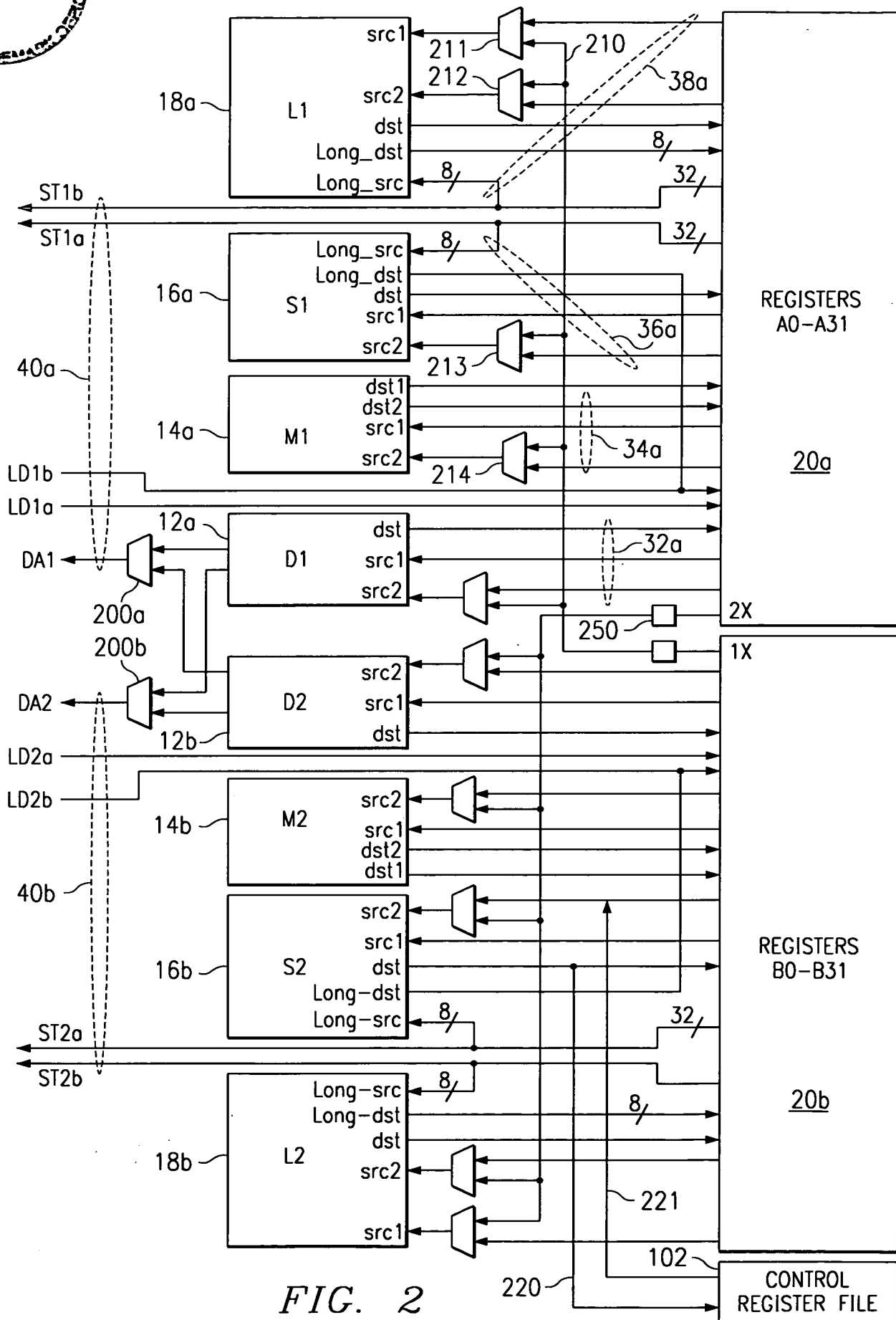


FIG. 1





OPERATIONS ON THE .L UNIT

31	29	28	27	23	22	18	17	13	12	11	5	4	3	2	1	0
CREG	Z	DST	SCR2	SRC1/CST	X	OP										
3	5	5	5	5	5	7										

FIG. 3A

OPERATIONS ON THE .M UNIT

31	29	28	27	23	22	18	17	13	12	11	7	6	5	4	3	2	1	0
CREG	Z	DST	SCR2	SRC1/CST	X	OP												
3	5	5	5	5	5	5												

FIG. 3B

OPERATIONS ON THE .D UNIT

31	29	28	27	23	22	18	17	13	12	7	6	5	4	3	2	1	0
CREG	Z	DST		SCR2		SRC1/CST		OP			1	0	0	0	0	S	P
3	5	5	5	5	5	5	6										

FIG. 3C

LOAD/STORE WITH 15-BIT OFFSET (ON THE .D UNIT)

31	29	28	27	23	22	8	7	6	4	3	2	1	0
CREG	Z	DST/SRC	UCST15	Y	LD/ST	1	1	S	P				
3	5	5	15	3	3								

FIG. 3D

LOAD/STORE 'BASER' + 'OFFSETR/CST' ON THE .D UNIT

31	29	28	27	23	22	18	17	13	12	9	8	7	6	4	3	2	1	0
CREG	Z	DST/SRC	BASE R	OFFSET R/UCST5	MODE	R	Y	LD/ST	0	1	S	P						
3	5	5	5	5	4													

FIG. 3E



OPERATIONS ON THE .S UNIT

31	29	28	27	23	22	18	17	13	12	11	6	5	4	3	2	1	0
CREG	Z		DST			SRC2		SRC1/CST	X		OP		0	0	0	0	S P
3			5					5			6						

FIG. 3F

ADDK ON THE .S UNIT

31	29	28	27	23	22	7	6	5	4	3	2	1	0
CREG	Z		DST					1	0	1	0	0	S P
3			5					16					

FIG. 3G

BITFIELD OPERATIONS (IMMEDIATE FORMS) ON THE .S UNIT

31	29	28	27	23	22	18	17	13	12	8	7	6	5	4	3	2	1	0
CREG	Z		DST			SRC2		CSTA		CSTB		OP	0	0	1	0	S	P
3			5					5			2							

FIG. 3H

MVK AND MVKH ON THE .S UNIT

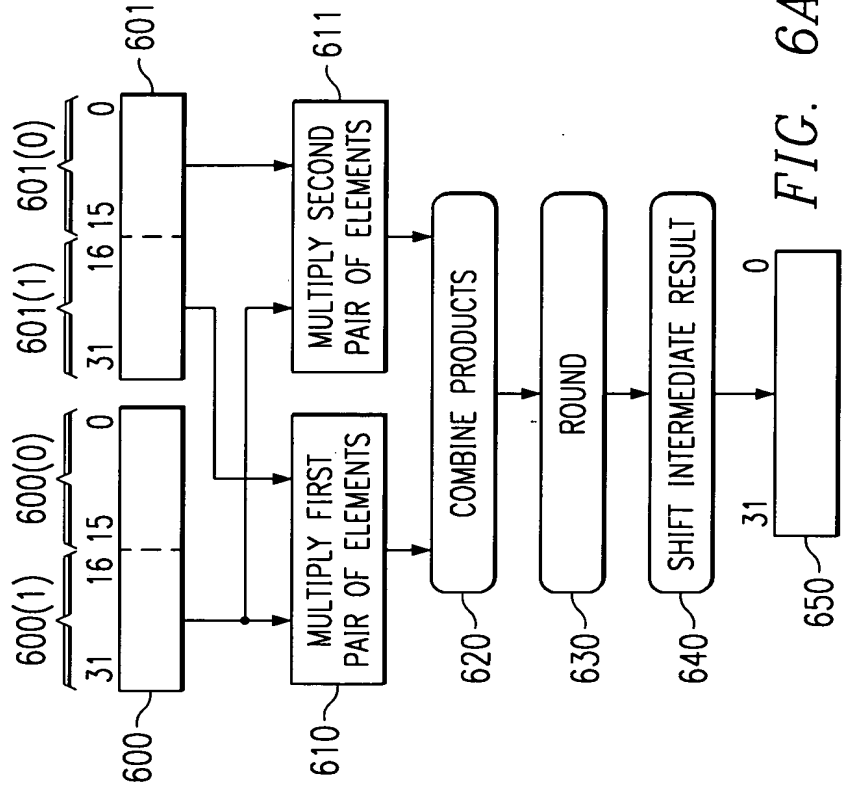
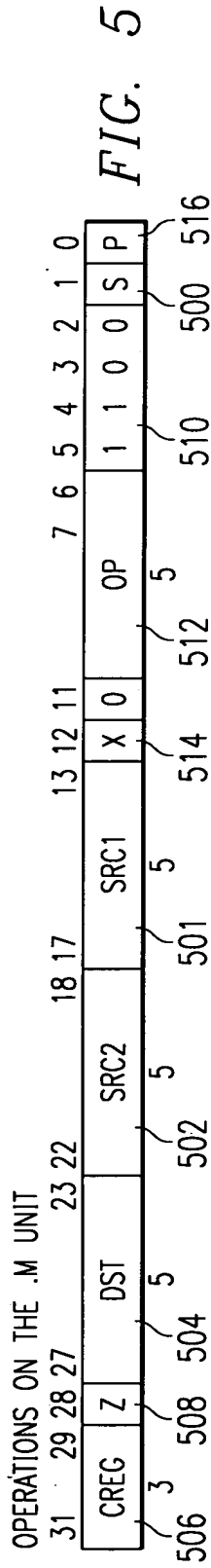
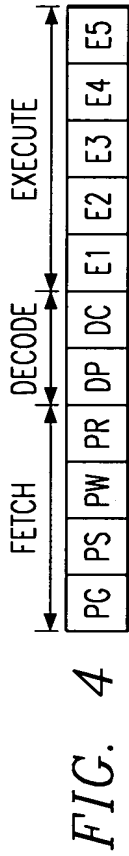
31	29	28	27	23	22	7	6	5	4	3	2	1	0
CREG	Z		DST					H	1	0	1	0	S P
3			5					16					

FIG. 3I

BCOND DISP ON THE .S UNIT

31	29	28	27		7	6	5	4	3	2	1	0
CREG	Z				CST		0	0	1	0	0	S P
3								21				

FIG. 3J



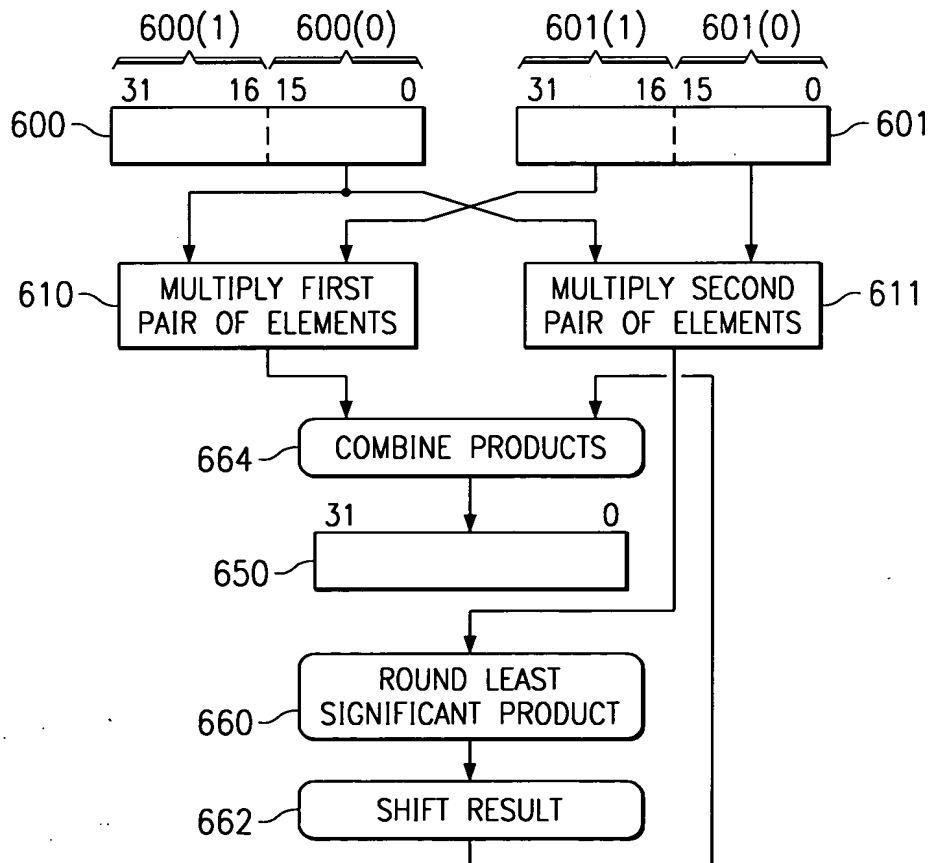
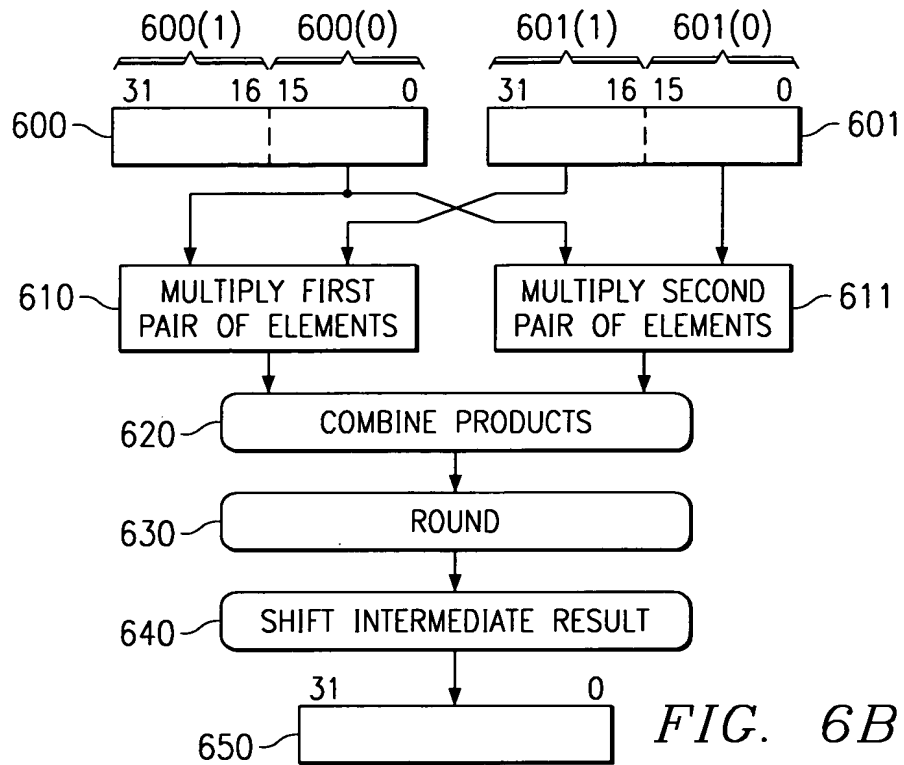


FIG. 7A

730a

730b

711

730b

MULT ARRAY(2)

711b

711a

PIPELINE REGISTERS

731b

MPY/AVG E2 LOGIC

AVG2/AVGU4/MPY 8/16/32 BIT ADDER

16/32 BIT ADDER

732b

PIPELINE REGISTERS

MPY E3 LOGIC

16/32/48 BIT ADDER

733c

PIPELINE REGISTERS

INCREMENTER

17 BIT ADDER

710

734

735

SATURATE LOGIC

SAT

DST1

ZERO1

DST2

ZERO2

730

AVG

BITC

NON-MPY E1 LOGIC

GMPY/MVD

700a

SWIZZLE NETWORK

ROT/SSHVL/SSHVR

PIPELINE REGISTERS

731a

ROT/SSHVL/SSHVR E2 LOGIC

700b

GMPY/MVD E2 LOGIC

732a

PIPELINE REGISTERS

700c

GMPY/MVD E3 LOGIC

733a

PIPELINE REGISTERS

(63:0)

(63:32)

(31:0)

DST1_MUX w/ ZERO_DETECT

DST2_MUX w/ ZERO_DETECT

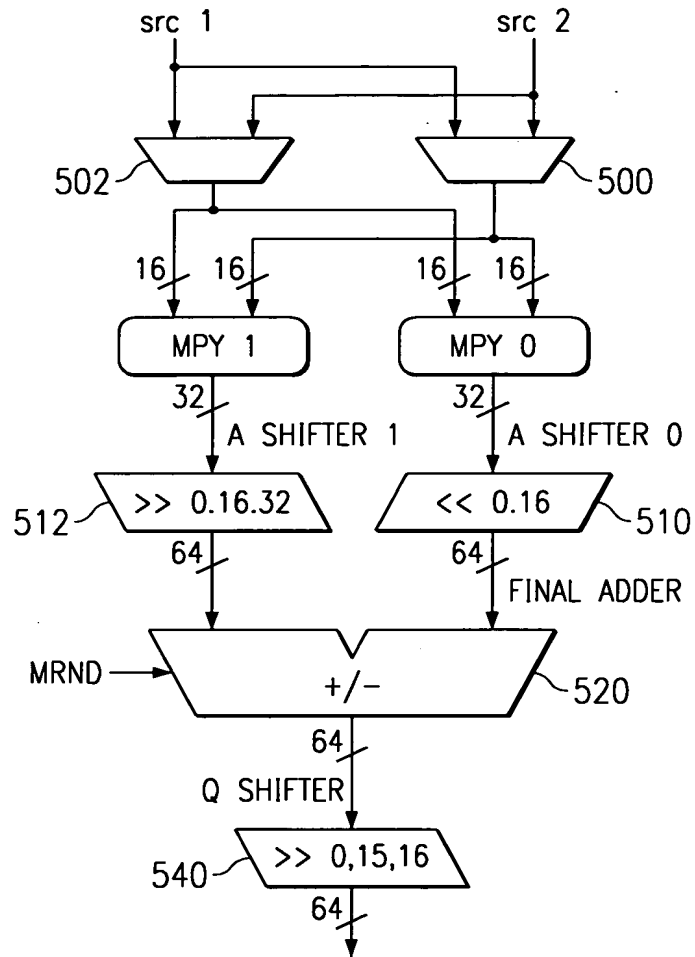
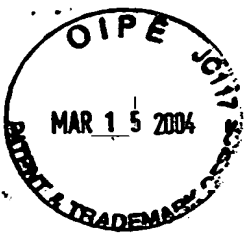


FIG. 7B

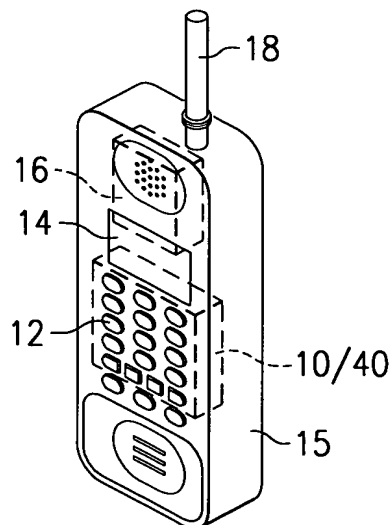


FIG. 8